

# **Notice of References Cited**

Application No.  
**09/069,054**

Applicant(s)  
**Richard CHAN et al.**

Examiner  
**A.M. Thompson**

Group Art Unit  
**2768**

Page 1 of 2

## **U.S. PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	4,758,745 ✓	07/19/88	Elgamal et al.	307	465
B	5,594,367 ✓	01/14/97	Trimberger et al.	326	41
C	5,835,751 ✓	11/10/98	Chen et al.	395	500
D	5,304,860 ✓	04/19/94	Ashby et al.	307	296.3
E	5,338,983 ✓	08/16/94	Agarwala	307	465
F	5,347,181 ✓	09/13/94	Ashby et al.	307	465
G	5,991,908 ✓	11/23/99	Baxter et al.	714	727
H	5,959,466 ✓	09/28/99	McGowan	326	39
I	5,874,834 ✓	02/23/99	New	326	39
J	5,469,003 ✓	11/21/95	Kean	326	39
K	5,452,231 ✓	09/19/95	Butts et al.	364	489
L	5,869,979 ✓	02/09/99	Bocchino	326	38
M	5,671,432 ✓	09/23/97	Bertolet et al.	395	800

## **FOREIGN PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

## **NON-PATENT DOCUMENTS**

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U	A. Aggarwal et al., Routing Architectures for Hierarchical Field Programmable Gate Arrays, IEEE International Conference on Computer Design: VLSI in Computers and Processors, pp. 475-478.	10/94
V	M. Karjalainen et al., Block Diagram Compilation and Graphical Editing of DSP Algorithms in the QuickSig System, IEEE Circuits and Systems, pp. 1057-1060	06/88
W	L.R. Ashby, Interface Techniques for Embedding Custom Mega Cells In A Gate Array, IEEE Custom Integrated Circuits Conference, pp. 23.5.1 - 23.5.4	05/93
X	A. El Gamal, An Architecture for Electrically Configurable Gate Arrays, IEEE Journal of Solid State Circuits, pp. 394-398	04/89

# **Notice of References Cited**

Application No.  
09/069,054

Applicant(s)  
Richard CHAN et al.

Examiner  
A.M. Thompson

Group Art Unit  
2768

Page 2 of 2

## **U.S. PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	5,878,051 ✓	03/02/99	✓ Sharma et al.	371	22.1
B	5,742,181 ✕	04/21/98	✓ Rush	326	41
C	5,224,056 ✕	06/29/93	✓ Chene et al.	364	490
D	5,894,565 ✕	04/13/99	✓ Furtek et al.	395	500
E	4,873,459 ✕	10/10/89	✓ El Gamal et al.	307	465
F	5,883,850 ✕	03/16/99	✓ Lee et al.	365	230.03
G					
H					
I					
J					
K					
L					
M					

## **FOREIGN PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

## **NON-PATENT DOCUMENTS**

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U	M. Agarwala et al., An Architecture for a DSP Field-Programmable Gate Array, IEEE Transactions on VLSI Systems, pp. 136-141. ✓	03/95
V		
W		
X		